CLAIMS

[Claim(s)]

[Claim 1] The A/D converter which carries out A/D conversion of the inputted picture signal, and the Horizontal Synchronizing signal separation circuit which takes out a synchronizing signal from said input picture signal, The Horizontal Synchronizing signal delay circuit delayed in the Horizontal Synchronizing signal extracted by this Horizontal Synchronizing signal separation circuit, The sampling clock generating circuit which generates the sampling clock for said A/D converters which synchronized with the Horizontal Synchronizing signal delayed by this Horizontal Synchronizing signal delay circuit, The picture signal incorporation circuit equipped with the digital memory which stores the picture signal by which A/D conversion was carried out with said A/D converter, and the amount control circuit of delay which controls the amount of delay of said Horizontal Synchronizing signal delay circuit based on the contents of this digital memory.

[Claim 2] The picture signal incorporation circuit equipped with the sampling clock generating circuit which generates the sampling clock for said A/D converters which synchronized with the Horizontal Synchronizing signal delayed by the A/D converter which carries out A/D conversion of the inputted picture signal, the Horizontal Synchronizing signal delay circuit delayed in the inputted Horizontal Synchronizing signal, and this Horizontal Synchronizing signal delay circuit, the digital memory which store the picture signal by which A/D conversion was carried out with said A/D converter, and the amount control circuit of delay which control the amount of said Horizontal Synchronizing signal delay circuit of delay based on the contents of this digital memory.

[Claim 3] The picture signal incorporation circuit equipped with the sampling clock generating circuit which generates the A/D converter which carries out A/D conversion of the inputted picture signal, and the sampling clock which synchronized with the inputted Horizontal Synchronizing signal, the sampling clock delay circuit delayed in the sampling clock generated by this sampling clock generating circuit, the digital memory which stores the picture signal by which A/D conversion was carried out with said A/D converter, and the amount control circuit of delay which control the amount of said sampling clock delay circuit of delay based on the contents of this digital memory.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the picture signal incorporation circuit which incorporates a picture signal in the digital memory for images.

[0002]

[Description of the Prior Art] It explains referring to drawing 7 about the configuration of the conventional picture signal incorporation circuit. Drawing 7 is the block diagram showing the conventional picture signal incorporation circuit.

[0003] In drawing 7 , 1 is an input picture signal, changes this input picture signal 1 into the digital image signal 3 with A/D converter 2, and stores it in the digital memory 4. Moreover, Horizontal Synchronizing signal 6 is extracted by the horizontal synchronization separation circuit 5 from the input picture signal 1, Horizontal Synchronizing signal 8 delayed by the Horizontal Synchronizing signal delay circuit 7 is inputted into the sampling clock generating circuit 9, a sampling clock 10 is generated, and it is used for A/D converter 2. Here, the amount of delay of the Horizontal Synchronizing signal delay circuit 7 is controllable by operating the amount control signal 13 of delay.

[0004] Next, actuation of the conventional picture signal incorporation circuit is explained. The input picture signal 1 superimposed on the synchronizing signal with the picture signal by which D/A conversion was carried out with the predetermined sampling rate (let this sampling rate be a dot clock.) is changed into the digital image signal 3 with a sampling clock 10 with A/D converter 2. At this time, a sampling clock 10 uses an equal for the dot clock of the input picture signal 1.

[0005] Moreover, a sampling clock 10 is delayed by the Horizontal Synchronizing signal delay circuit 7 in Horizontal Synchronizing signal 6 which separated the input picture signal 1 by the horizontal synchronization separation circuit 5, and delayed Horizontal Synchronizing signal 8 is used for it, and by the sampling clock generating circuit 9, it is building it so that it may synchronize with delay Horizontal Synchronizing signal 8. The contents of the digital memory 4 are taken out to a monitor 17 by D/A-converter 15 grade, and it checks whether the phase of the dot clock of the input picture signal 1 and the phase of a sampling clock 10 are correct.

[0006] When both phases do not suit, the sharpness of the image on a monitor 17 is lost, or a noise occurs. In that case, by changing the amount control signal 13 of delay, the amount of delay of delayed Horizontal Synchronizing signal 8 is changed, and the phase of a sampling clock 10 oscillated by the sampling clock generating circuit 9 synchronizing with it is changed. Adjustment of this amount control signal 13 of delay is performed looking at a monitor 17.

[0007]

[Problem(s) to be Solved by the Invention] Since the conventional picture signal incorporation circuit is constituted as mentioned above, in order to double the phase of a dot clock, and the phase of a sampling clock 10, it needed to check with the monitor 17 and the amount control signal 13 of delay needed to be adjusted with the help. Therefore, there was a trouble that it had to reset up with a help one by one to change of the trouble that the amount of adjustments varies, and phases, such as a temperature drift, by the monitor and the difference in those who adjust.

[0008] This invention aims at obtaining the picture signal incorporation circuit with which the phase of a dot clock and a sampling clock can be doubled automatically, without having been made in order to cancel the above troubles, and seeing a monitor.

[0009]

[Means for Solving the Problem] The picture signal incorporation circuit concerning claim 1 of this invention is equipped with the means hung up over a degree.

[1] The A/D converter which carries out A/D conversion of the inputted picture signal.

[2] The Horizontal Synchronizing signal separation circuit which takes out a synchronizing signal from said input picture signal.

[3] The Horizontal Synchronizing signal delay circuit delayed in the Horizontal Synchronizing signal extracted by this Horizontal Synchronizing signal separation circuit.

[4] The sampling clock generating circuit which generates the sampling clock for said A/D converters which synchronized with the Horizontal Synchronizing signal delayed by this Horizontal Synchronizing signal delay circuit.

[5] Digital memory which stores the picture signal by which A/D conversion was carried out with said A/D converter.

[6] The amount control circuit of delay which controls the amount of delay of said Horizontal Synchronizing signal delay circuit based on the contents of this digital memory.

[0010] The picture signal incorporation circuit concerning claim 2 of this invention is equipped with the means hung up over a degree.

[1] The A/D converter which carries out A/D conversion of the inputted picture signal.

[2] The Horizontal Synchronizing signal delay circuit delayed in the inputted Horizontal Synchronizing signal.

[3] The sampling clock generating circuit which generates the sampling clock for said A/D converters which synchronized with the Horizontal Synchronizing signal delayed by this Horizontal Synchronizing signal delay circuit.

[4] Digital memory which stores the picture signal by which A/D conversion was carried out with said A/D converter.

[5] The amount control circuit of delay which controls the amount of delay of said Horizontal Synchronizing signal delay circuit based on the contents of this digital memory.

[0011] The picture signal incorporation circuit concerning claim 3 of this invention is equipped with the means hung up over a degree.

[1] The A/D converter which carries out A/D conversion of the inputted picture signal.

[2] The sampling clock generating circuit which generates the sampling clock which synchronized with the inputted Horizontal Synchronizing signal.

[3] The sampling clock delay circuit delayed in the sampling clock generated by this sampling clock generating circuit.

[4] Digital memory which stores the picture signal by which A/D conversion was carried out with said A/D converter.

[5] The amount control circuit of delay which controls the amount of delay of said sampling clock delay circuit based on the contents of this digital memory.

[0012]

[Function] In this invention, the phase error of a dot clock and a sampling clock is detected from the digital image data incorporated in digital memory by the amount control circuit of delay, and the amount of delay is changed. That is, the amount control circuit of delay analyzes the digital image data on digital memory, a Horizontal Synchronizing signal delay circuit or a sampling clock delay circuit is controlled, and the amount of delay is made to change so that the phase of a dot clock and a sampling clock may suit.

[0013]

[Example] It explains below example 1., referring to drawing 1 about the configuration of the example 1 of this invention. Drawing 1 is the block diagram showing the example 1 of this invention.

[0014] In drawing 1 , conventionally, since [which was mentioned above] it is the same as that of a circuit, the input picture signal 1 – a sampling clock 10, and the amount control signal 13 of delay give the same sign to a considerable part, and omit those detailed explanation.

[0015] The digital image data 11 are taken out by the digital memory 4, it analyzes in the amount control circuit 12 of delay which consists of CPUs etc., the amount control signal 13 of delay is built, and the Horizontal Synchronizing signal delay circuit 7 is controlled.

[0016] Next, it explains, referring to drawing 2 , drawing 3 , and drawing 4 about actuation of the example 1 of this invention. Drawing 2 is drawing showing the image data when incorporating the m–th line by the example 1 in memory twice. Moreover, drawing 3 is drawing showing the relation between the different number by the example 1, and the amount of delay. Furthermore, drawing 4 is a flow chart which shows actuation of an example 1.

[0017] Memory of the m–th line of the input picture signal 1 is carried out about twice, and the pixel data between 2 times are compared. When shown in drawing 2 , a pixel which is different two places by the 1st time and the 2nd time exists. If the number of this different part changes the amount of delay and recarries out memory twice in certain amount of delay +b as it is shown in drawing 3 , it will be set to 0 of the minimum value. The amount of delay is changed so that the amount of delay may be **ed to positive/negative from the current amount 0 of delay and the different number may become small.

[0018] Drawing 4 showed the flow chart which calculates the amount of delay used as the

number from which min differs. First, it asked for the different number in the amounts L1 and L2 (=L1+deltaL) of delay (steps 18-19), and the amount of delay was changed in the which direction, or it has judged at step 20.

[0019] In step 25, the amount of delay is changed in the direction whose different number decreases. And it judges [whether the minimum value was exceeded and] at step 26. L value of before at the time of the different number exceeding the minimum value increasing serves as the amount of delay from which the phase error of a dot clock and a sampling clock serves as min.

[0020] The approach in this case is subject [to becoming the value which changes with noises generated according to a phase error even if it samples the same Rhine again]. It is also possible to perform same processing noting that it differs when it judges with not all values, but a moderate threshold is prepared and the difference beyond a certain value occurs since it may be based on a steady noise when sampling again and becoming a different value.

[0021] Since the example 1 of this invention amends the amount of delay so that the amount control circuits 12 of delay, such as CPU, may analyze the digital image data on the digital memory 4, the Horizontal Synchronizing signal delay circuit 7 may be controlled about the circuit which incorporates a picture signal in the digital memory 4 and the phase of a dot clock and a sampling clock may suit as mentioned above, it does so the effectiveness that a picture signal can be incorporated with high precision.

[0022] In addition, the digital memory which stores the picture signal by which A/D conversion was carried out with A/D converter 2 by several lines is sufficient as the digital memory 4.

[0023] As shown in example 2. drawing 5 , when the input picture signal 1 is not overlapped on a Horizontal Synchronizing signal (i.e., when Horizontal Synchronizing signal 6a is given from the exterior), the horizontal synchronization separation circuit 5 is unnecessary, and the Horizontal Synchronizing signal delay circuit 7 is delayed in Horizontal Synchronizing signal 6a inputted from the outside.

[0024] Although delay control of the Horizontal Synchronizing signal was carried out in example 3. above-mentioned each example, as shown in drawing 6 , even if it carries out delay control of the sampling clock, the same operation effectiveness is done so. That is, sampling clock generating circuit 9a generates a sampling clock synchronizing with Horizontal Synchronizing signal 6a inputted from the outside, and sampling clock delay circuit 7a is delayed based on the amount control signal 13 of delay in a sampling clock.

[0025]

[Effect of the Invention] As explained above, this invention detects the phase error of a dot clock and a sampling clock by analyzing the image data on digital memory, and since it constituted so that the amount of delay might be amended, it does so the effectiveness that incorporation of an accurate picture signal becomes possible.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the example 1 of this invention.

[Drawing 2] It is drawing showing the image data when incorporating the m-th line in memory twice based on the example 1 of this invention.

[Drawing 3] It is drawing showing the relation between the different number by the example 1 of this invention, and the amount of delay.

[Drawing 4] It is the flow chart which shows actuation of the example 1 of this invention.

[Drawing 5] It is the block diagram showing the example 2 of this invention.

[Drawing 6] It is the block diagram showing the example 3 of this invention.

[Drawing 7] It is the block diagram showing the conventional picture signal incorporation circuit.

[Description of Notations]

1 Input Picture Signal
2 A/D Converter
3 Digital Image Signal
4 Digital Memory
5 Horizontal Synchronization Separation Circuit
6 Horizontal Synchronizing Signal
7 Horizontal Synchronizing Signal Delay Circuit
8 Delayed Horizontal Synchronizing Signal
9 Sampling Clock Generating Circuit
10 Sampling Clock
11 Digital Image Data
12 The Amount Control Circuit of Delay
13 The Amount Control Signal of Delay

[Translation done.]